REMARKS

In the Office Action mailed July 28, 2006 claims 1, 4–17 and 20–27 were rejected. By the present response, claim 17 has been amended. No new subject matter has been added. Upon entry of the amendment, claims 1, 4-17 and 20-27 will be pending in the application. Reconsideration and allowance of all pending claims are requested.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1, 4-7, 10-12, 14 and 15 under 35 U.S.C. § 102(b) as being anticipated by Soderbarg et al. (U.S. Patent No. 6,063,693, hereinafter "Soderbarg"). Applicants submit that all of the claims are distinguishable over Soderbarg. In particular, independent claim 1 specifically recites planarizing a semiconductor wafer, which is neither taught nor suggested by Soderbarg.

Independent Claim 1 cannot be anticipated by Soderbarg

Soderbarg fails to teach planarizing a semiconductor wafer surface

Claim 1 specifically recites a method for optical and electrical isolation between adjacent integrated devices comprising *planarizing* the semiconductor wafer surface by removing the portion of the optically isolating material above the exposed surface of the semiconductor wafer.

As set forth in the Application:

> Figure 6 shows the wafer cross section after the step of surface planarization. This step substantially flattens top surface 210 of the wafer by removing the excess polysilicon on top of the wafer. According to one embodiment of the present invention, the wafer may be subjected to a wet or dry thermal oxidation process where the portion of polysilicon on the top surface reacts with a water steam or oxygen and turns into oxide. The resulting oxide layer may then be removed with wet chemicals such as hydrofluoric acid (HF). Or the excessive polysilicon may be removed directly by anisotropic plasma etching or chemical mechanical polishing (CMP). The polysilicon removal process may also etch away part of silicon dioxide layer 206 left on the top surface of the wafer. However

> most of the trench-coating silicon dioxide layer 206 and trench-filling polysilicon layer 208 will be intact. After planarization of the top surface, the wafer is now ready for subsequent fabrication processes.
>
> Application, page 9, para [0032] (emphasis added).

On the other hand, Soderbarg discloses:

> When the polysilicon layer 6 is etched away from the wafer surface to expose the second insulation layer 9 a downward vertical step 8 remains over the trench 1. This is caused by over-etching of the polysilicon layer 6. This over-etching is required to ensure that all the polysilicon on top of the planar surface 3 is removed.
>
> The surface of the polysilicon layer 6 remaining in the trench 1 is then oxidized to form an isolating oxide cover 10 over the trench as shown in FIG. 1e. The silicon substrate 2 in the regions 12 where the oxide walls of the trenches 1 have sloping tops which incline downwardly towards the inside of the trench has only a thin covering of polysilicon 6.
>
> Soderbarg, col. 3, lines 21-33 (emphasis added).

Further, Soderbarg discloses:

> In an embodiment of the method according to the present invention for forming planar trenches, as illustrated in FIGS. 2a-2d, a trench is etched in the substrate in a conventional manner, for example, as described above with respect to FIGS. 1a-1d.
>
> Soderbarg, col. 3, lines 61-65.

Thus, Soderbarg teaches over-etching of the polysilicon layer so as to provide space for an isolating oxide cover. Further, Soderbarg discloses trenches having sloping tops. Clearly, Soderbarg *does not* teach or even suggest planarizing a semiconductor wafer surface in a trench.

Hence, Applicants respectfully submit that Soderbarg cannot anticipate claim 1 or claims 4-7, 10-12, 14 and 15 depending therefrom and request withdrawal of the rejections under 35 U.S.C. § 102.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 8, 9, 17 and 20-27 under 35 U.S.C. § 103(a) as being unpatentable over Soderbarg in view of Guo (U.S. Patent No. 6,894,357, hereinafter "Guo").

By the present response, independent claim 17 has been amended to include the recitation "and planarized by removing a portion of the optically isolating material above an exposed surface of the substrate."

Claim 17

Amended independent claim 17 specifically recites a microelectronic device comprising at least one trench in the substrate, wherein the at least one trench physically separates the at least two integrated devices, and the inside of the at least one trench is coated with an electrically insulating material, filled with an optically isolating material that is conformally deposited and *planarized* by removing a portion of the optically isolating material above an exposed surface of the substrate.

On the contrary, Soderbarg discloses:

> In order to isolate components in integrated circuits from each other refilled trench structures have been developed.

Soderbarg, col. 1, lines 8-10.

As discussed above, Soderbarg fails to teach or even suggest trench structures that are planarized. On the contrary, Soderbarg teaches overetching a polysilicon layer to accommodate an isolating oxide cover over the trench. Further, as cited above, Soderbarg discloses a trench with a sloping top. Guo does nothing to obviate this deficiency of Soderbarg.

Hence, claim 17 is believed to be clearly patentable over Soderbarg and Guo.

Dependent claims (from 1 and 17)

Claims 8, 9 and 20-27 depend directly or indirectly on allowable base claims 1 and 17. Accordingly, these claims are believed to be clearly patentable at least by virtue of their dependency from the allowable base claims.

Claim 13

The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Soderbarg in view of Ring (U.S. Patent Application Publication No. 2002/0066960, hereinafter "Ring").

Claim 13 depends directly from an allowable base claim 1. Accordingly, claim 13 is believed to be clearly patentable at least by virtue of dependency from the allowable base claim.

Claim 16

The Examiner rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Soderbarg in view of Witek et al. (U.S. Patent No. 6,146,970, hereinafter "Witek").

Claim 16 depends directly from an allowable base claim 1. Accordingly, claim 16 is believed to be clearly patentable at least by virtue of dependency from the allowable base claim.

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully request allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 10/30/2006

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